DATA SHEET

SAA5233
Dual standard PDC decoder

Objective specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Dual standard PDC decoder SAA5233

FEATURES

- Digital data slicer
- Acquisition and decoding of VPS data (EBU PDC System A)
- Acquisition and decoding of Teletext packet 8/30/2 data (EBU PDC System B)
- Separate storage of VPS data and packet 8/30/2 allowing dual standard PDC decoders
- I²C-bus interface with automatic word address increment
- Programmable interrupt for data received
- Programmable error level detection
- Single +5 V power supply.

GENERAL DESCRIPTION

The SAA5233 is a dual standard Program Delivery Control (PDC) decoder, allowing the reception and decoding of both VPS data (EBU PDC System A) and Teletext packet 8/30/2 data (EBU PDC System B). It is intended for use in European video recorders which are manually programmed, so that they receive broadcast real time switching signals for accurate timing of program recording.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	45	mA
f_{clk}	crystal input frequency	–	27	–	MHz
V_{sync}	CVBS sync voltage amplitude	0.1	0.3	0.6	V
$V_{vid(p-p)}$	CVBS video voltage amplitude (peak-to-peak value)	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5233P	16	DIP16	plastic	SOT38-1
SAA5233T	20	SO20L	plastic	SOT163-1

BLOCK DIAGRAM

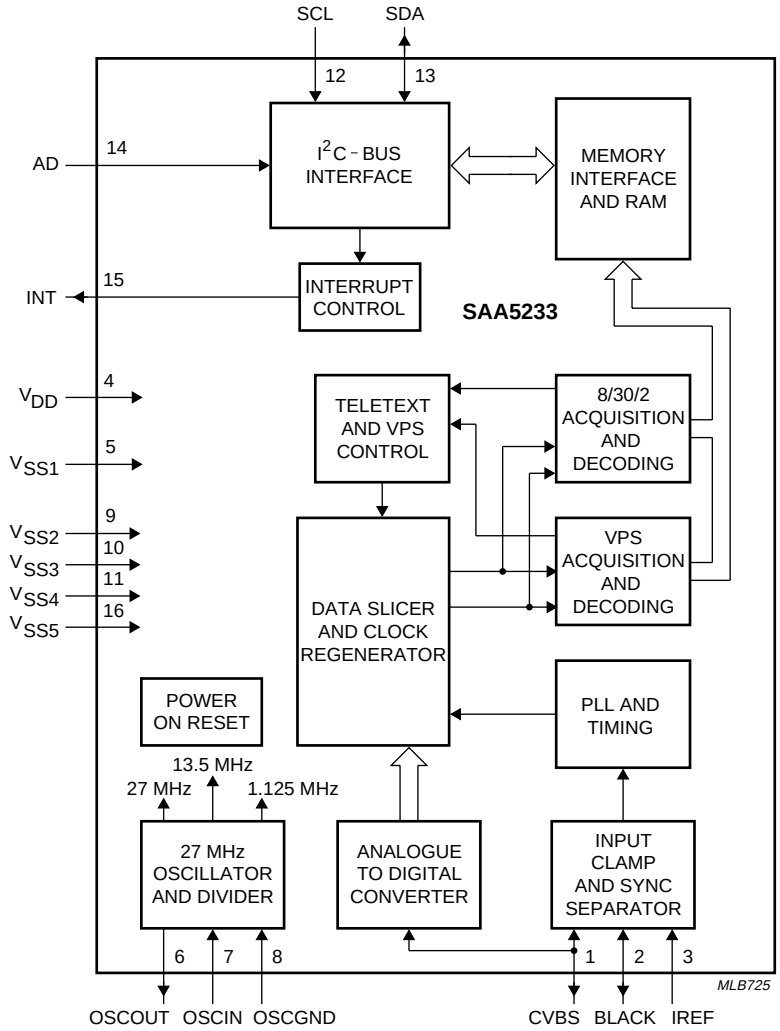


Fig.1 Block diagram; pin numbers for DIP16.

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16	SO20L	
CVBS	1	1	composite video input
BLACK	2	2	video black level storage pin
n.c.	–	3	not connected
IREF	3	4	reference current input
V_{DD}	4	5	+5 V supply
V_{SS1}	5	6	0 V ground 1 (main ground pin)
OSCOUT	6	7	27 MHz crystal oscillator output
n.c.	–	8	not connected
OSCIN	7	9	27 MHz crystal oscillator input
OSCGND	8	10	27 MHz crystal oscillator ground
V_{SS2}	9	11	0 V ground 2; connect to V_{SS1}
V_{SS3}	10	12	0 V ground 3; connect to V_{SS1}
n.c.	–	13	not connected
V_{SS4}	11	14	connect to V_{SS1} in normal operation
SCL	12	15	serial clock open-drain input for I^2C-bus
SDA	13	16	serial data open-drain input/output for I^2C-bus
i.c.	–	17	internally connected; do not connect in normal operation
AD	14	18	programmable I^2C-bus address bit input
INT	15	19	interrupt open-drain output
V_{SS5}	16	20	connect to V_{SS1} in normal operation

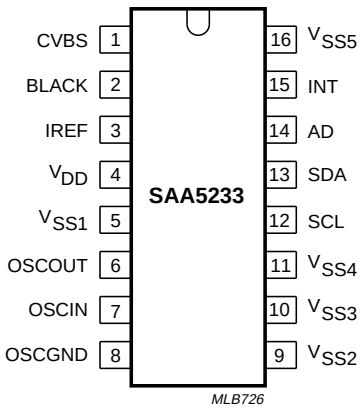


Fig.2 Pin configuration; DIP16.

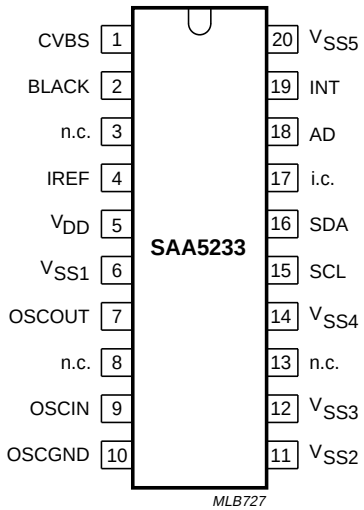


Fig.3 Pin configuration; SO20L.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	+6.5	V
V_{Imax}	maximum input voltage (any input)	–0.3	V_{DD} + 0.3	V
V_{Omax}	maximum output voltage (any output)	–0.3	V_{DD} + 0.3	V
I_{IOmax}	maximum DC input or output diode current	–	±20	mA
I_{Omax}	maximum output current (any output)	–	±10	mA
T_{amb}	operating ambient temperature	–20	+70	°C
T_{stg}	storage temperature	–55	+125	°C

QUALITY AND RELIABILITY

This device will meet the requirements of the *"Philips Semiconductors General Quality Specification SNW-FQ-611E"* in accordance with *"Quality Reference Pocketbook (order number 9398 510 34011)"*. The principal requirements are as shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot.

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <100 ppm
Electrical	cumulative target: <100 ppm

Group B

Table 2 Processability tests (by package family).

TEST	REQUIREMENTS(1)
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Group C

Table 3 Reliability tests (by process family).

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1500 FPM; equivalent to <100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias (1000 hours, 85 °C, 85% RH or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 4 Reliability tests (by device type).

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V; 100 pF; 1.5 kΩ	<15% LTPD
	ESD Machine model 200 V; 200 pF; 0 Ω	<15% LTPD
	latch-up 100 mA; $1.5 \times V_{DD}$ (absolute maximum)	<15% LTPD

Note to Tables 1 to 4.

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current		–	30	45	mA
Inputs						
CVBS						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
$V_{dat(text)}$	Teletext data voltage amplitude		0.30	0.46	0.70	V
$V_{dat(vps)}$	VPS data voltage amplitude		0.30	0.50	0.70	V
Z_{source}	source impedance		–	–	250	Ω
Z_I	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
V_{IREF}	input reference voltage		–	$0.5V_{DD}$	–	V
AD						
V_{IL}	LOW level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	μA
C_I	input capacitance		–	–	10	pF
SCL						
V_{IL}	LOW level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	μA
C_I	input capacitance		–	–	10	pF
f_{clk}	clock frequency		0	–	100	kHz
t_r	input rise time	$0.3V_{DD}$ to $0.7V_{DD}$	–	–	1000	ns
t_f	input fall time	$0.7V_{DD}$ to $0.3V_{DD}$	–	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
INT (OPEN-DRAIN OUTPUT)						
V_{PU}	pull-up voltage at pin		–	–	V_{DD}	
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	4.0	mA
C_L	load capacitance		–	–	400	pF
t_f	output fall time	C_L = 100 pF; $0.7V_{DD}$ to $0.3V_{DD}$	–	–	100	ns
Inputs/Outputs						
BLACK						
C_{black}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
SDA (OPEN-DRAIN OUTPUT)						
V_{IL}	LOW level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	400	pF
t_r	input rise time	$0.3V_{DD}$ to $0.7V_{DD}$	–	–	1000	ns
t_f	input fall time	$0.7V_{DD}$ to $0.3V_{DD}$	–	–	300	ns
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
t_f	output fall time	C_L = 400 pF; $0.7V_{DD}$ to $0.3V_{DD}$	–	–	200	ns
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
V_{osc}	oscillator voltage amplitude (peak-to-peak value)		–	1.0	–	V
G_v	small signal voltage gain		–	1.0	–	
C_I	input capacitance		–	–	10	pF
C_{fb}	feedback capacitance		–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.4)						
f_{clk}	SCL clock frequency		0	–	100	kHz
t_{BUF}	bus free time between a STOP and START		4.7	–	–	µs
$t_{HD;STA}$	repeated START hold time	note 1	4.0	–	–	µs
t_{LOW}	SCL clock LOW time		4.7	–	–	µs
t_{HIGH}	SCL clock HIGH time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START		4.7	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;DAT}$	data set-up time		250	–	–	ns
t_r	SDA, SCL input rise time	$0.3V_{DD}$ to $0.7V_{DD}$	–	–	1 000	ns
t_f	SDA, SCL input fall time	$0.7V_{DD}$ to $0.3V_{DD}$	–	–	300	ns
$t_{SU;STO}$	set-up time for STOP		4.0	–	–	µs

Note

1. After this time the first clock pulse is generated.

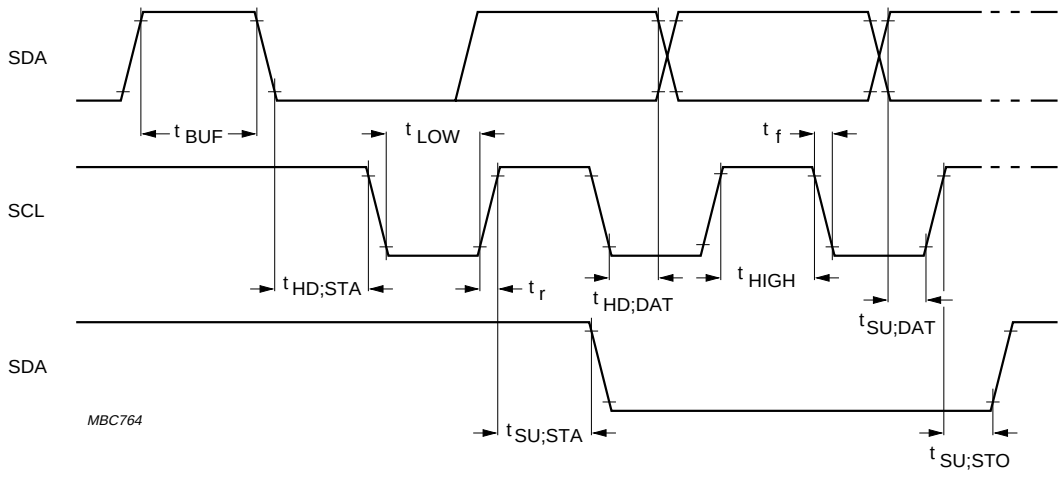


Fig.4 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Control of device

The function of the device is controlled via the I²C-bus. Pin AD provides a choice of two alternative addresses.

The PDC acquisition section requires little software control apart from enabling the interrupts which occur when data is found. Interrupts can be enabled for either Teletext packet 8/30/2 or VPS and both can be enabled to allow for the presence of both standards being transmitted on the same TV channel. The interrupt register is accessed as address 01 WRITE, see Section “Register 01: Interrupt (reset state X00X XXXX)”.

When an interrupt is signalled, a bit is set in the status register to indicate its source. Information about the received PDC data is given in the status register D5 and D6. The microcontroller must service the ‘data received’ interrupts within 40 ms (VPS) or 200 ms (Teletext packet 8/30/2), since new data may be written after this period. The status register is accessed as address 00 READ; see Section “Register 00:Control/Status (reset state XXX0 XX00)”. When the status register has been read the data received flags and interrupt signal are reset.

Data of both types is constantly received and stored, but can be selectively acquired by setting bits D1 and D0 of the control register. This allows acquisition of only Teletext packet 8/30/2 on every VBI line or only VPS data on every VBI line. The control register is accessed as address 00 WRITE, see Section “Register 00:Control/Status (reset state XXX0 XX00)”.

Storage of PDC data

The PDC data memory is accessed at address 02 (HEX) to 31 (HEX). The exact addresses of Teletext packet 8/30/2 and VPS data is shown in Table 5.

TELETEXT DATA

The Teletext packet 8/30/2 data is stored after hardware Hamming correction. There are 4 data bits stored in the lower nibble of each byte in address 11 (HEX) to 1D (HEX); see Table 13, in the order shown in Table 5. The status message, which is odd parity coded, is stored as a byte which represents a Teletext character in address 1E (HEX) to 31 (HEX); see Table 14.

VPS DATA

The VPS data from Line 16 is stored in register address 02 (HEX) to 0F (HEX) in the order shown in Table 5. VPS data is biphase decoded and stored with 4 data bits stored in the lower nibble of each byte, in the same way as Teletext packet 8/30/2 data; see Tables 11 and 12. In addition to the VCR data, Word 4 (Program Source Identification, ASCII sequential) is stored, which may be useful for future applications.

The stored data is read via the I²C-bus in the normal way. Multiple reception/majority error correction of the data is the responsibility of the control software, the device simply stores the data as transmitted after Hamming or biphase decoding. As both VPS and Teletext packet 8/30/2 signals are stored separately, it is possible to deal with future situations where both EBU PDC System A and EBU PDC System B transmissions may be present on the same TV channel, the defaults and level of service being chosen by the software control.

Error indication

Indication of errors in the received data is given in two ways and is programmable by setting bit D4 in the control register.

The first is a flag to indicate Hamming or biphase errors and is stored with the related data in bit 0 of the upper nibble of the data byte.

The second is no interrupt which is sent to the microcontroller but the data signal quality bit (D7) is set.

The level of interrupt is controlled by the Interrupt Error Level bit which is D4 of the control register. If this bit is not set then an interrupt only occurs if an error free line of either Teletext packet 8/30/2 or VPS data is received and stored in RAM. If this bit is set then an interrupt occurs if the correct framing code and Teletext packet header 8/30/2 is found, or the correct start code for VPS data is found. The data is then stored in the RAM with any errors indicated in the upper nibble. This may be used by more sophisticated software, which could decide the importance of an error in a particular nibble.

I²C-bus interface

FEATURES

- Standard I²C-bus slave transceiver
- Operates from 0 to 100 kHz
- Acknowledge function is performed
- Auto-increment between registers and direct addressing
- Selectable I²C-bus slave address dependent on address pin AD.

Register map

The data received when address locations 00 (HEX) to 31 (HEX) are read or written is shown in Table 5.

Table 5 Register map.

ADDRESS (HEX)	DATA[1]	ADDRESSING
00	control/status	direct
01	interrupt	direct
02	VPS B5	direct/auto-increments to 03
03	VPS B5	direct/auto-increments to 04
04	VPS B11	direct/auto-increments to 05
05	VPS B11	direct/auto-increments to 06
06	VPS B12	direct/auto-increments to 07
07	VPS B12	direct/auto-increments to 08
08	VPS B13	direct/auto-increments to 09
09	VPS B13	direct/auto-increments to 0A
0A	VPS B14	direct/auto-increments to 0B
0B	VPS B14	direct/auto-increments to 0C
0C	VPS B15	direct/auto-increments to 0D
0D	VPS B15	direct/auto-increments to 0E
0E	VPS B4	direct/auto-increments to 0F
0F	VPS B4	stop value
10	–	direct
11	8/30/2 B13	direct/auto-increments to 12
12	8/30/2 B14	direct/auto-increments to 13
13	8/30/2 B15	direct/auto-increments to 14
14	8/30/2 B16	direct/auto-increments to 15
15	8/30/2 B17	direct/auto-increments to 16
16	8/30/2 B18	direct/auto-increments to 17
17	8/30/2 B19	direct/auto-increments to 18
18	8/30/2 B20	direct/auto-increments to 19
19	8/30/2 B21	direct/auto-increments to 1A
1A	8/30/2 B22	direct/auto-increments to 1B
1B	8/30/2 B23	direct/auto-increments to 1C
1C	8/30/2 B24	direct/auto-increments to 1D
1D	8/30/2 B25	direct/auto-increments to 1E
1E	status message	direct/auto-increments to 1F
:	:	direct/auto-increments
31	status message	stop value

Note

1. For the address range 02H to 0FH, even addresses hold the least significant nibble and odd addresses hold the most significant nibble. BXX refers to byte definitions, EBU specification of the domestic video PDC system.

Register 00:Control/Status (reset state XXX0 XX00)

Register 00 is split into two parts. The control part (WRITE only) consisting of bits D4, D1 and D0 and status part (READ only) consisting of bits D7 to D5.

Table 6 Register 00.

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	IEL	–	–	ACQ 8/30/2	ACQ VPS
DSQ	8/30/2 RF	VPS RF	–	–	–	–	–

Table 7 Register 00 bit description.

SYMBOL	BIT	FUNCTION
IEL	D4	Interrupt Error Level. When logic 0, signal only completely valid data lines from Teletext packet 8/30/2 received and VPS received flags. When logic 1, signal valid framing code and Teletext packet header 8/30/2 received or valid start codeword for VPS received.
ACQ 8/30/2 ACQ VPS	D1 D0	Acquire 8/30/2. Acquire VPS. Allows selective decoding of either Teletext packet 8/30/2 data or VPS data. If both are set to the same value the system automatically selects the format being transmitted (see Table 8).
DSQ	D7	Data Signal Quality. When logic 1, good Teletext or VPS data signal is being received. When logic 0, no Teletext or VPS data signal is being received.
8/30/2 RF	D6	8/30/2 Received Flag. When logic 1, and IEL (D4) = logic 0 an error-free Teletext packet 8/30/2 has been received, Hamming decoded and stored in the RAM. When logic 1, and IEL(D4) = logic 1 a Teletext packet with a valid framing code and 8/30/2 header has been received, Hamming decoded and stored in RAM. When logic 0 no Teletext packet 8/30/2 data received.
VPS RF	D5	VPS Received Flag. When logic 1, and IEL(D4) = logic 0, an error-free VPS data line has been received, biphase decoded and stored in the RAM. When logic 1, and IEL(D4) = logic 1 a VPS data line with valid start code has been received, biphase decoded and stored in RAM. When logic 0 no VPS data received.

Table 8 Selection of Teletext packet 8/30/2 data or VPS data.

ACQ 8/30/2	ACQ VPS	FUNCTION
0	0	use automatic selection algorithm for line 16
0	1	acquire only VPS data on every VBI line
1	0	acquire only 8/30/2 data on every line 16
1	1	use automatic selection algorithm for line 16

Register 01: Interrupt (reset state X00X XXXX)

Register R01 is WRITE only.

Table 9 Register 01.

D7	D6	D5	D4	D3	D2	D1	D0
–	8/30/2 IE	VPS IE	–	–	–	–	–

Table 10 Register 01 bit description.

SYMBOL	BIT	FUNCTION
8/30/2 IE	D6	8/30/2 Interrupt Enable. This allows the reception of Teletext packet 8/30/2 data to be signalled on the INT pin. When logic 0 reception of Teletext packet 8/30/2 data is not signalled on INT pin. When logic 1 reception of Teletext packet 8/30/2 data is signalled on INT pin.
VPS IE	D5	VPS Interrupt Enable. This allows the reception of VPS data to be signalled on the INT pin. When logic 0 reception of VPS data is not signalled on INT pin. When logic 1 reception of VPS data is signalled on INT pin.

Register 02 to 0F (HEX): VPS data bytes

A single VPS data bytes is stored as two memory bytes, the least significant nibble of both memory bytes is the data making up the single VPS data byte. The most significant nibble of each memory byte is used to indicate a biphase error in the least significant nibble. This is indicated by the least significant bit being set, the top three bits are not used and are fixed to logic 0 (see Table 11).

Table 11 VPS data bytes.

ADDRESS (HEX)	REGISTER	DATA
02	VPS B5 least significant nibble	0000 1100[1]
03	VPS B5 most significant nibble	0000 0101[1]

Note

1. Equivalent to VPS B5 0101 1100 (MSB to LSB).

Table 12 Register 02.

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	BIPHASE ERROR BIT	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

Register 11 to 1D (HEX): Teletext packet 8/30/2 data bytes

Data is stored as single bytes. The four least significant bits represent the data. The fifth bit if set indicates a Hamming error in the stored data. The top three bits of the byte are not used and are fixed to logic 0.

Table 13 Register 11.

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	HAMMING ERROR BIT	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

Register 1E to 31D (HEX): Status display message

Data is stored as bytes which represent a Teletext character. The data is odd parity checked, if a parity error occurs this causes the byte not to be written to the RAM. The MSB is not used and is fixed to logic 0.

Table 14 Register 11.

D7	D6	D5	D4	D3	D2	D1	D0
–	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

I²C-bus slave address

The slave address for the device can take one of two values dependent on the state of the input pin AD.

Table 15 Device address.

AD	SLAVE ADDRESS
0	0010 001X(1)
1	0010 000X(1)

Note

1. Where X is the R/$\overline{W}$ bit.

I²C-bus increment

The I²C-bus will also increment between registers as listed in Table 16

Table 16 Increment between registers**.**

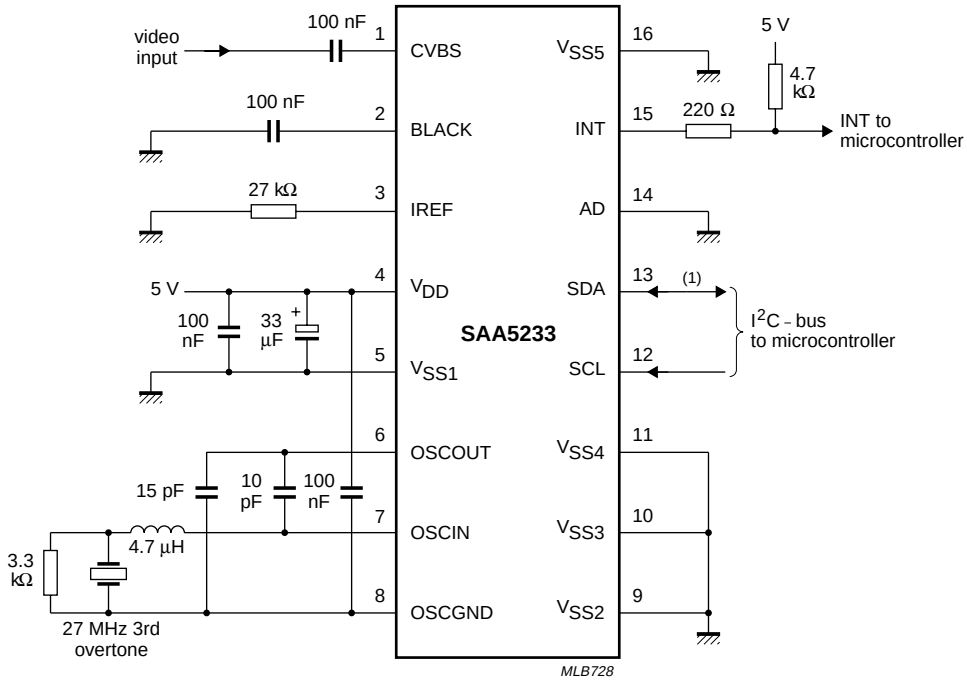
ADDRESS	CONTENTS
02 to 0F (HEX)	VPS data bytes
11 to 31 (HEX)	Teletext packet 8/30/2 data bytes and Status display message

Addressing any register in either of these ranges will initialize an increment until the final stop value provided each byte is acknowledged by the receiver.

Initialization during power-up

The device has an internal power-on reset unit which is used to reset the I²C-bus interface to be a slave transceiver. It also initializes the device to receive only completely valid Teletext packet 8/30/2 and VPS data. The interrupt signals for both Teletext packet 8/30/2 and VPS are disabled.

APPLICATION INFORMATION



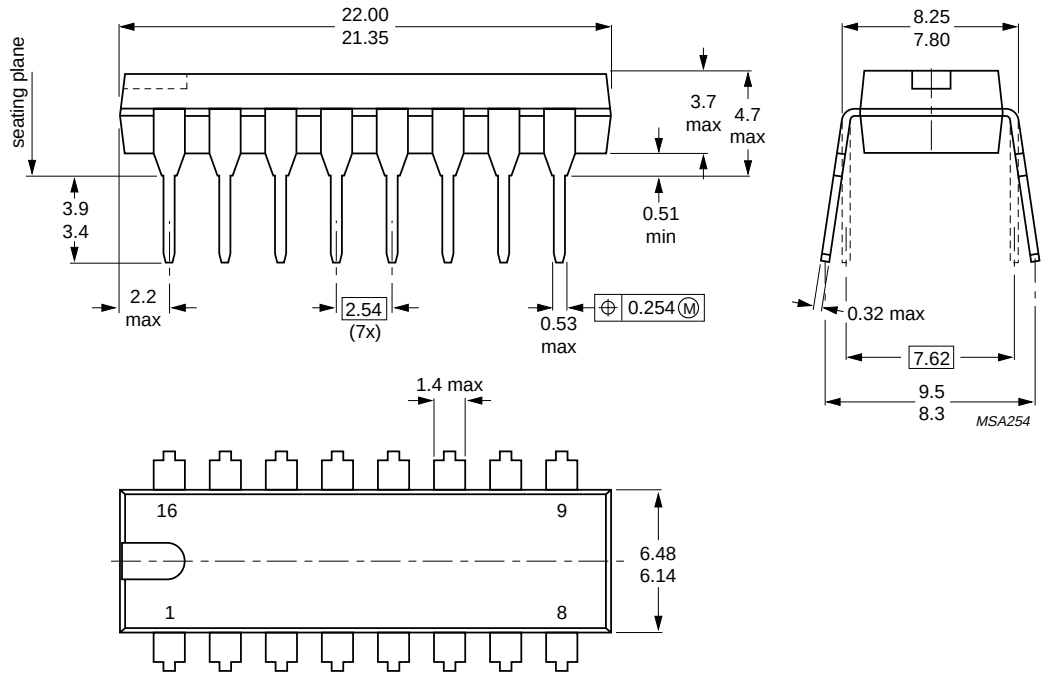
(1) I²C-bus address 0010 001R/$\overline{W}$.

Fig.5 Application diagram; DIL16.

Table 17 Crystal characteristics.

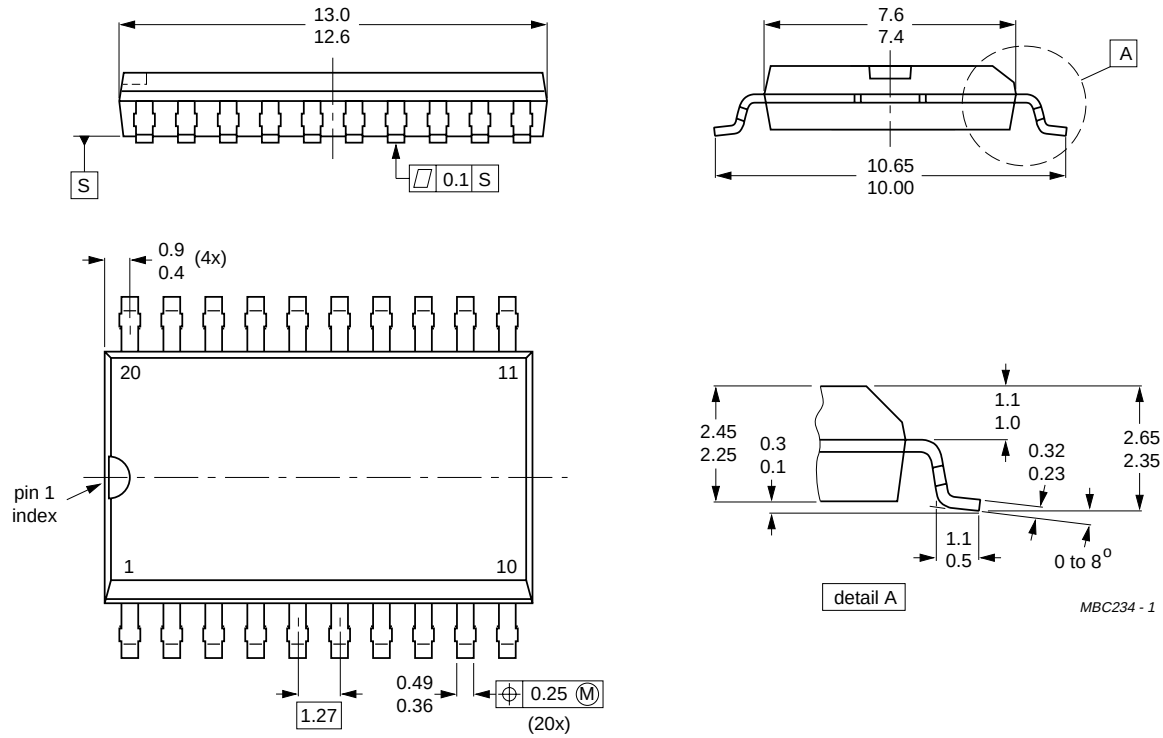
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)				
C1	series capacitance	1.7	–	pF
C0	parallel capacitance	5.2	–	pF
C_L	load capacitance	20	–	pF
R_r	resonance resistance	–	50	Ω
R1	series resistance	20	–	Ω
X_a	ageing	–	$\pm 5 \times 10^{-6}$	$year^{-1}$
X_j	adjustment tolerance	–	$\pm 25 \times 10^{-6}$	
X_d	drift	–	$\pm 25 \times 10^{-6}$	

PACKAGE OUTLINES



Dimensions in mm.

Fig.6 Plastic dual in-line package; 16 leads (300 mil); DIP16, SOT38-1.



Dimensions in mm.

Fig.7 Plastic small outline package; 20 leads; large body; SO20L, SOT163-1.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low-voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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